Amendments to the Specification:

Please amend paragraph [0011] as follows:

[0011] In the present invention, a tuning circuit comprises a voltage controlled oscillator for generating a first clock signal, where the voltage controlled oscillator includes an inductive element, a variable capacitive element coupled to the inductive element and a bank of switched capacitors coupled to the inductive element and the variable capacitive element. A frequency divider generates a second clock signal responsive to the first clock signal and a predetermined divisor. Frequency control circuitry controls the variable capacitive element responsive to a frequency difference between ~~the first and~~ a reference signal and the second clock ~~signals~~ signal. Logic circuitry determines an initial control word to configure the trimming capacitor bank using a search responsive to a desired frequency and determines whether the initial control word should either remain the same or change to an adjacent control word.

Please amend paragraph [0032] as follows:

[0032] Figure 5 illustrates a frequency diagram of a first scenario, where there is a relatively small overlap in frequency range between adjacent codes to the bank 21. In the illustrated embodiment, bank 21 includes seven capacitors 24, hence the control word can have a value between zero (all capacitors disabled) and seven (all capacitors enabled). In the illustrated embodiment of Figure 5, there is about a 50% overlap between adjacent control words; i.e., the midpoint of the frequency range (f_{mid}, assuming that the analog control voltage to the varactor 14 is set to the middle of its capacitive range during calibration) for a particular control word is at about the same level as the lower bound of the frequency range ([[f_{max}]] f_{min}) for the preceding control word and at about the same level as the upper bound of the frequency range (f_{max}) for the subsequent control word.